TS32GSSD25-M
TS64GSSD25-M
TS128GSSD25-M

2.5” Solid State Disk

Description

Due to smaller size (fit the standard dimensions of 2.5” IDE Hard Disk Drives), huge capacity, high speed, and low power consumption, Solid State Disk is perfect replacement storage device for PCs, Laptops, gaming systems, and handheld devices.

Placement

Features

- RoHS compliant
- Fully compatible with devices and OS that support the IDE standard (44-Pin, pitch = 2.00 mm)
- Non-volatile Flash Memory for outstanding data retention
- Built-in ECC (Error Correction Code) functionality and wear-leveling algorithm ensures highly reliable of data transfer
- Supports up to Ultra DMA Mode 6
- Shock resistance

Dimensions

Side	Millimeters	Inches
A	100.30 ± 0.40	3.949 ± 0.016
B	69.85 ± 0.20	2.750 ± 0.008
C	7.40 ± 0.15	0.292 ± 0.004

Specifications

Physical Specification		
Form Factor		2.5-inch HDD
Storage Capacities		32 GB to 128 GB
Dimensions (mm)	**Length**	100.3 0 ± 0.40
	Width	69.85 ± 0.20
	Height	7.40 ± 0.15
Input Voltage		5V ± 10%
Weight		55g ± 5g
Connector		44-Pin standard IDE/ATA connector (Pitch 2.0 mm)

Environmental Specifications	
Operating Temperature	0 ℃ to 70 ℃
Storage Temperature	- 40 ℃ to 85 ℃

Power Requirements			
Input Voltage		5V ± 5%	
Mode		**TYP (mA)**	**TYP (W)**
Power Consumption (DC 5V @25℃)	**Write**	88.2	0.44
	Read	94.6	0.47
	Idle	1.5	0.07

Interface Specification	
Jumper Settings	Master/Slave/Cable-select Settings
ATA Compatibility	ATA/ATAPI 8
	UDMA Modes 6

Performance		
Model P/N	**Sequential Read**(Max.)	**Sequential Write**(Max.)
TS32GSSD25-M	80 MB/s	30 MB/s
TS64GSSD25-M	80 MB/s	30 MB/s
TS128GSSD25-M	80 MB/s	30 MB/s

* Note : 25 ℃, according to 44 pin to 40 pin IDE transferring cable test on GIGABYTE GA-965P-DS3, 1GB RAM, IDE interface support UDMA, Windows® XP Version 2002 SP2, benchmark utility HDBENCH (version 3.4006), copied file 100MB

Actual Capacity				
Model P/N	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
TS32GSSD25-M	62,521,344	16,383	16	63
TS64GSSD25-M	125,206,528	16,383	16	63
TS128GSSD25-M	252,411,904	16,383	16	63

Reliability	
Data Reliability	Supports BCH ECC 15 bits in 512 bytes
Data Retention	10 years

Vibration	
Operating	3.0G, 5 - 800Hz
Non-Operating	3.0G, 5 - 800Hz

* Note: Reference to the IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

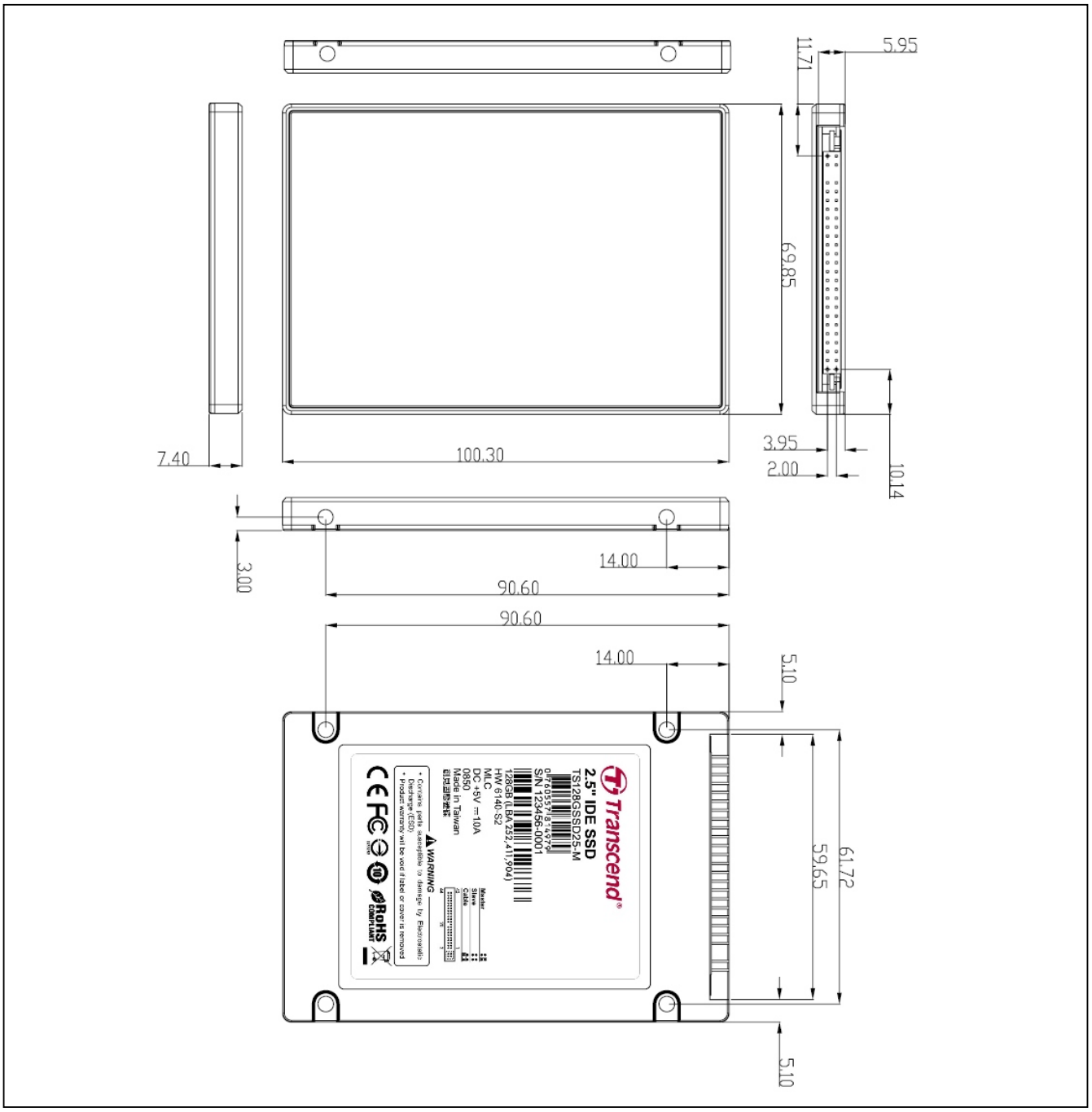
Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms

*Note: Reference to the IEC 60068-2-27 Testing procedures; Operating-Half-sine wave, 1500g, 0.5ms, 3 times/dir., total 18 times.

Regulations	
Compliance	CE, FCC and BSMI

Package Dimensions

Below figure illustrates the Transcend 2.5” Solid State Disk. All dimensions are in mm.

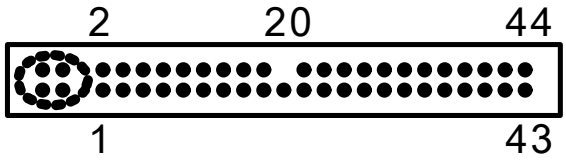


***Note: Tighten mounting screws with no more than 1.0Kg-cm (0.07ft-lbs) of torque.**

Pin Assignments

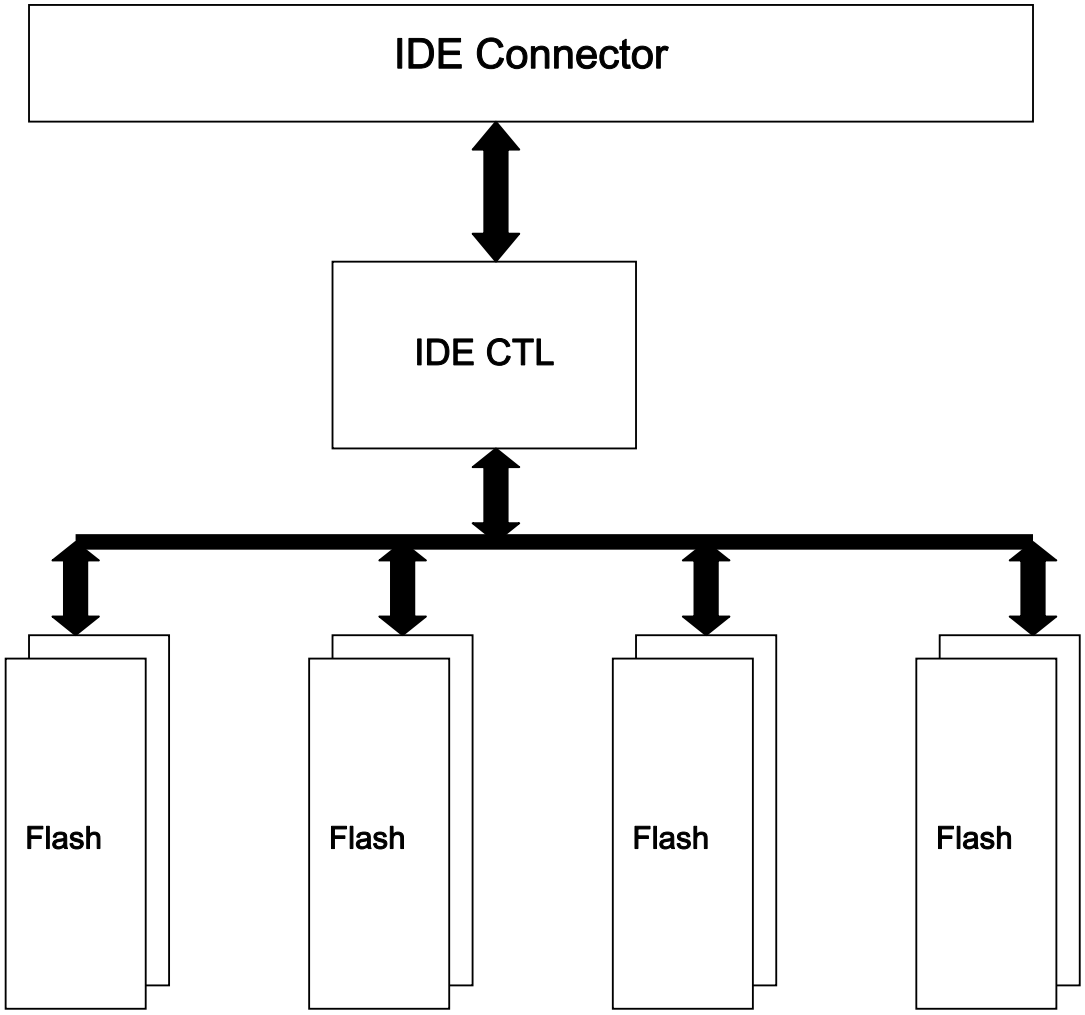
Pin No.	Pin Name	Pin No.	Pin Name
01	-RESET	02	GND
03	DD7	04	DD8
05	DD6	06	DD9
07	DD5	08	DD10
09	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	KEY-PIN (OPEN)
21	DMARQ	22	GND
23	-DIOW : STOP	24	GND
25	-DIOR : -HDMARDY : HSTROBE	26	GND
27	IORDY : DDMARDY : DSTROBE	28	CSEL
29	-DMACK	30	GND
31	INTRQ	32	IOCS16B
33	DA1	34	-PDIAG : -CBLID
35	DA0	36	DA2
37	-CS0	38	-CS1
39	-DASP	40	GND
41	VCC	42	VCC
43	GND	44	NC (No Connect)

Pin Layout



Master Mode Slave Mode Cable Select

Block Diagram



Reliability

Wear-Leveling algorithm

The controller supports static/dynamic wear leveling. When the host writes data, the controller will find and use the block with the lowest erase count among the free blocks. This is known as dynamic wear leveling. When the free blocks' erase count is higher than the data blocks', it will activate the static wear leveling, replacing the not so frequently used user blocks with the high erase count free blocks.

ECC algorithm

The controller uses BCH15 ECC algorithm per 512 bytes. BCH15 can correct up to 15 random error bits within 512 data bytes.

Bad-block management

When the flash encounters ECC failed, program fail or erase fail, the controller will mark the block as bad block to prevent the used of this block and caused data lost later on.

Support ATA/ATAPI Command List

Support ATA/ATAPI Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
READ DMA	C8h	DMA
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	CAh	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Mode Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data
SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-In
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out

■ General Feature Set

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

➢ **Identify Device Information Default Value**

Word Address	Default value	Total Bytes	Data Field Type Information
0	0x044Ah	2	General configuration
1	0x3FFF	2	Default number of cylinders
2	0x0000	2	Reserved
3	0x000F	2	Default number of heads
4-5	0x02400000	4	Obsolete
6	0x003F	2	Default number of sectors per track
7 - 8	0x0F0FF7BF	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0x0000	2	Obsolete
10 - 19	0xXXXXh	20	Serial number in ASCII (Right justified)
20-21	0x00020002	4	Obsolete
22	0x0000	2	Obsolete
23 - 26	0xXXXXh	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27 - 46	0xXXXXh	40	Model number in ASCII (Left justified). Big Endian Byte Order in Word.
47	0x8001	2	Maximum number of sectors on Read/Write Multipl command
48	0x0000	2	Reserved
49-50	0xXXXXh	4	Capabilities
51-52	0x00000200	4	PIO data transfer cycle timing mode
53	0x0007	2	Field validity
54	0xXXXXh	2	Current numbers of cylinders
55	0xXXXXh	2	Current numbers of heads
56	0xXXXXh	2	Current sectors per track
57 - 58	0xXXXXh	4	Current capacity in sectors (LBAs) (Word57 = LSW , Word58 = MSW)
59	0x0100	2	Multiple sector setting
60 - 61	0xXXXXh	4	Total number of sectors addressable in LBA Mode

Word Address	Default value	Total Bytes	Data Field Type Information
62	0x0000	2	Reserved
63	0x0007	2	Multiword DMA transfer Supports MDMA Mode 0, 1 and 2
64	0x0003	2	Advanced PIO modes supported
65	0x0078	2	Minimum Multiword DMA transfer cycle time per word
66	0x0078	2	Recommended Multiword DMA transfer cycle time
67	0x0078	2	Minimum PIO transfer cycle time without flow control
68	0x0078	2	Minimum PIO transfer cycle time with IORDY flow control
69 –74	0x0000	18	Reserved
75	0x0000	2	Queue depth
76-79	0x0000	8	Reserved for Serial ATA
80	0x0800	2	Major version number (ATAPI-7)
81	0x0000	2	Minor version number
82	0x742B	2	Command sets supported 0
83	0x5100	2	Command sets supported 1
84	0x4002	2	Command sets supported 2
85	0xXXXXh	2	Command set/feature enabled 0
86	0xXXXXh	2	Command set/feature enabled 1
87	0xXXXXh	2	Command set/feature enabled 2
88	0xXX7F	2	Ultra DMA mode supported and selected Default: Ultra DMA mode 6
89	0x0003	2	Time required for Security erase unit completion
90	0x0000	2	Time required for Enhanced security erase unit completion
91	0x0000	2	Current Advanced power management value
92	0x0000	3	Master Password Revision Code
93	0x604F 0x6F00 0x603F	2	• Hardware reset result (Master only) • Hardware reset result (Slave only) • Hardware reset result (Master w/ slave present)
94	0x0000h	2	Current Automatic acoustic management value
95	0x0000h	2	Stream Minimum Request Size
96	0x0000h	2	Streaming Transfer Time -- DMA
97	0x0000h	2	Streaming Access Latency – DMA and PIO
98-99	0x0000h	4	Streaming Performance Granularity
100-103	0x0000h	8	Maximum user LBA for 48-bit Address feature set
104	0x0000h	2	Streaming Transfer Time – PIO
105	0x0000h	2	Reserved
106	0x0000h	2	Physical sector size / Logical sector size
107	0x0000h	2	Inter-seek delay for ISO 7779 standard acoustic testing

Word Address	Default value	Total Bytes	Data Field Type Information
108-111	0x0000h	8	World wide name
112-115	0x0000h	8	Reserved for a 128-bit world wide name
116	0x0000h	2	Reserved for technical report
117-118	0x0000h	4	Logical sector size
119-126	0x0000h	16	Reserved
127	0x0000h	2	Removable Media Status Notification feature set support
128	0x0001	2	Security Status
129-159	0xXXXXh	62	Vendor specific
160	0x0000h	2	CFA Power mode
161-175	0x0000h	2	Reserved for assignment by the Compact Flash
176-205	0x0000h	60	Current media serial number
206-254	0x0000h	98	Reserved
225	0x0000h	2	Integrity word

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

SET FEATURES (EFh)

This command set parameter to Features register and set drive’s operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

WRITE DMA (CAh)
Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE MULTIPLE (C5h)
This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE SECTOR(S) (30h)
Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify “00h” to write 256 sectors.

NOP (00h)
The device shall respond with command aborted. For devices implementing the Overlapped feature set, subcommand code 00h in the Features register shall abort any outstanding queue. Subcommand codes 01h through FFh in the Features register shall not affect the status of any outstanding queue.

READ BUFFER (E4h)
The READ BUFFER command enables the host to read a 512-byte block of data.

WRITE BUFFER (E8h)
This command enables the host to write the contents of one 512-byte block of data to the device’s buffer.

■ Power Management Feature Set

CHECK POWER MODE (E5h or 98h)
The host can use this command to determine the current power management mode.

IDLE (E3h or 97h)
This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h or 95h)
This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

SLEEP (E6h or 99h)
This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

STANDBY (E2h or 96h)
This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h or 94h)
This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately.

■ Security Mode Feature Set

SECURITY SET PASSWORD (F1h)

This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

Security set Password data content

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set user password 1=set master password
	Bits 1-7	Reserved	
	Bit 8	Security level	0=High 1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY UNLOCK (F2h)

This command disable LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

Security Unlock information

Word	Content		
0	Control word		
	Bit 0	Identifier	0=compare user password 1=compare master password
	Bits 1-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

SMART Feature Set

Transcend IDE SSD supports the SMART command set and define some vendor-specific data to report spare/bad block numbers in each memory management unit. Individual SMART commands are identified by the value placed in the Feature register. Table shows these Feature register values.

Value	Command
D0h	SMART READ DATA
D2h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D4h	SMART EXECUTE OFF-LINE IMMEDIATE
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS
DAh	SMART RETURN STATUS

SMART DISABLE OPERATIONS

B0h with a Feature register value of D9h.Disables the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on.

Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error.

This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles.

SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

B0h with a Feature register value of D2h.Enables or disables the attribute value autosave function. This command specifies whether the current attribute values are automatically saved to the drive when it changes the mode. This setting is maintained when the power is turned on and off.

SMART ENABL OPERATIONS

B0h with a Feature register value of D8h.Enables the SMART function. This setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters

SMART EXECUTE OFF-LINE IMMEDIATE

B0h with the content of the Features register equal to D4h. This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode.

SMART RETURN STATUS

B0h with a Feature register value of DAh.This command causes the device to communicate the reliability status of the device to the host. If a threshold exceeded condition is not detected by the device, the device shall set the LBA Mid register to 4Fh and theLBA High register to C2h. If a threshold exceeded condition is detected by the device, the device shall set the LBA Mid register to F4h and the LBA High register to 2Ch.

SMART Read Data

B0h with the content of the Features register equal to D0h. This command returns the Device SMART data structure to the host.

SMART DATA Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the

Byte	F / V	Description
0 - 1	X	Revision code
2 - 114	X	Vendor specific
115-116	V	Power cycle count of the device
117-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364 - 365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368 - 369	F	SMART capability
370	F	Error logging capability • 7-1 Reserved • 0 1 = Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375 - 385	R	Reserved
386 - 395	F	Firmware Version/Date Code
396 - 397	F	Number of initial invalid block (396 = MSB, 397 = LSB)
398 - 399	V	Number of run time bad block (398 = MSB, 399 = LSB)
400 - 406	F	Reserved
407 - 415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418 – 419	**V**	**Number of spare block**
420	F	Reserved
421 – 423	**V**	**Average erase count**
424 – 425	**V**	**Number of child pair**
426 – 428	**V**	**Maximum erase count**
429 – 431	**V**	**Minimum erase count**
432 – 445	F	Reserved
446 – 510	X	Vendor specific
511	V	Data structure checksum

Note:

F = content (byte) is fixed and does not change.

V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.

X = content (byte) is vendor specific and may be fixed or variable. R = content (byte) is reserved and shall be zero.

N = Nth Management Unit

*4 Byte value: [MSB] [2] [1] [LSB]

Host Protected Area Feature Set

A reserved area for data storage outside the normal operating system file system is required for several specialized applications. Systems may wish to store configuration data or save memory to the device in a location that the operating systems cannot change. The optional Host Protected Area feature set allows a portion of the device to be reserved for such an area when the device is initially configured.

Ultra DMA data transfer

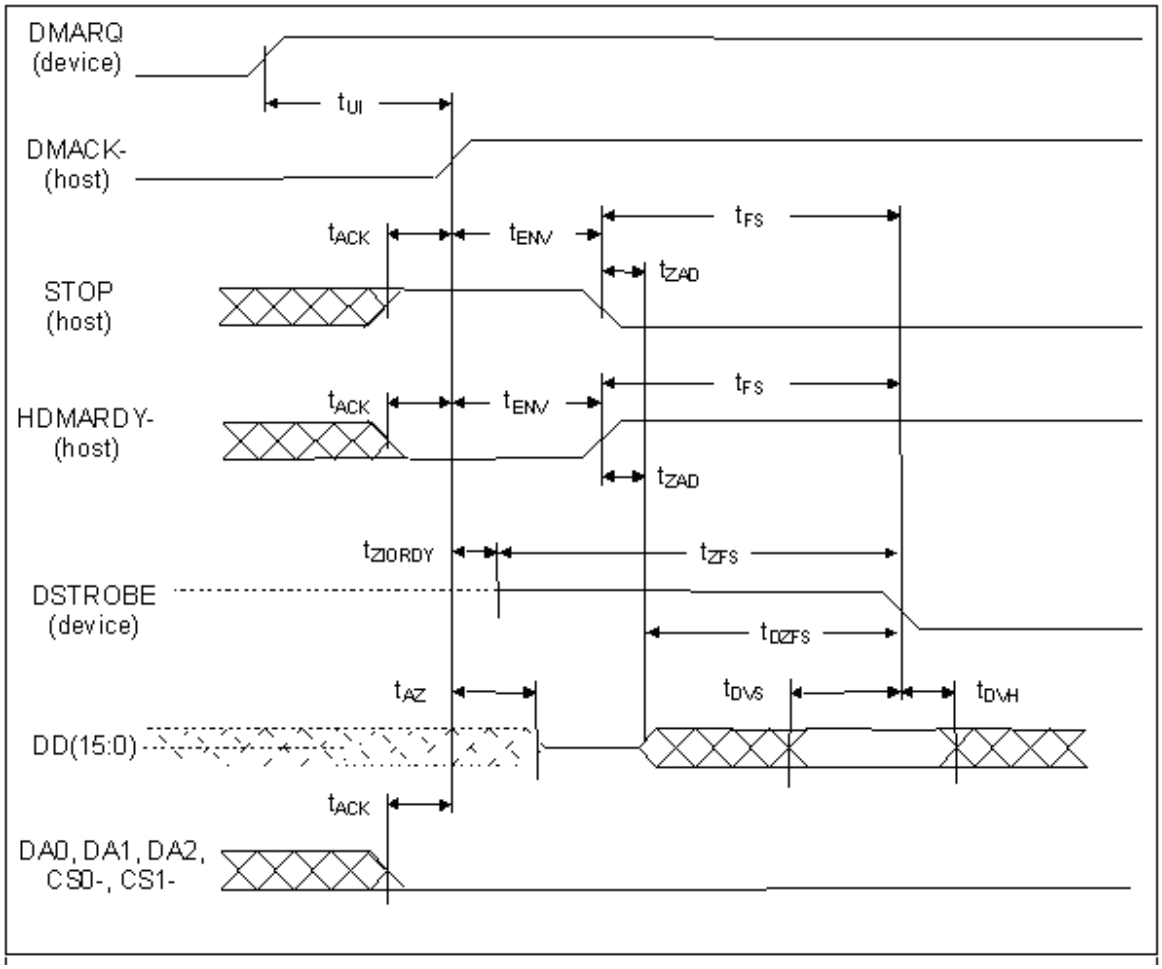
Ultra DMA data burst timing requirements

Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Mode 5 (in ns)		Mode 6 (in ns)		Measurement location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		40		30		Sender
t_{CYC}	112		73		54		39		25		16.8		13.0		Note 3
t_{2CYC}	230		153		115		86		57		38		29		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		2.6		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		3.5		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		4.0		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		4.0		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		10.0		Host
t_{ZFS}	0		0		0		0		0		35		25		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		17.5		Sender
t_{FS}		230		200		170		130		120		90		80	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	0	60	Note 4
t_{MLI}	20		20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	20	50	Host
t_{RFS}		75		70		60		60		60		50		50	Sender
t_{RP}	160		125		100		100		100		85		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		50		Sender

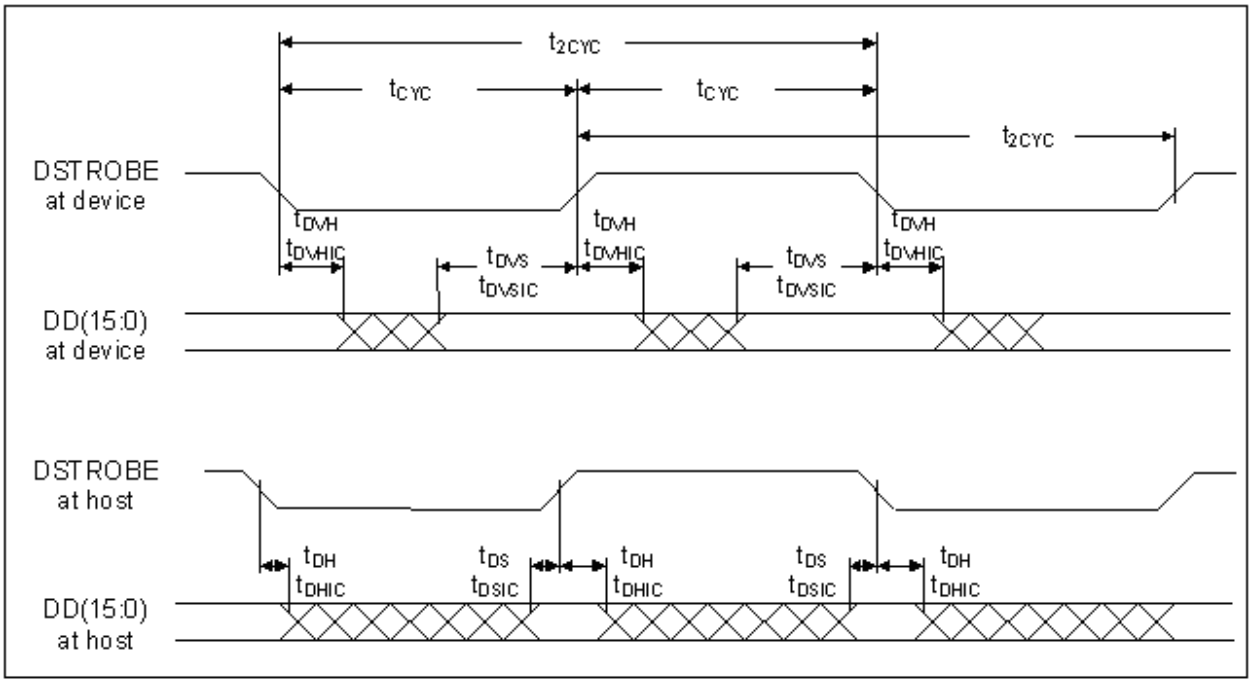
Ultra DMA data burst timing descriptions

Name	Comment
$t_{2CYCTYP}$	Typical sustained average two cycle time
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)
t_{CS}	CRC word setup time at device
t_{CH}	CRC word hold time device
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK- negation)
t_{CVH}	CRC word valid hold time at sender (from DMACK- negation until CRC may become invalid)
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	Limited interlock time
t_{MLI}	Interlock time with minimum
t_{UI}	Unlimited interlock time
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	Minimum delay time required for output
t_{ZAD}	drivers to assert or negate (from released)
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)
t_{IORDYZ}	Maximum time before releasing IORDY
t_{ZIORDY}	Minimum time before driving IORDY
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

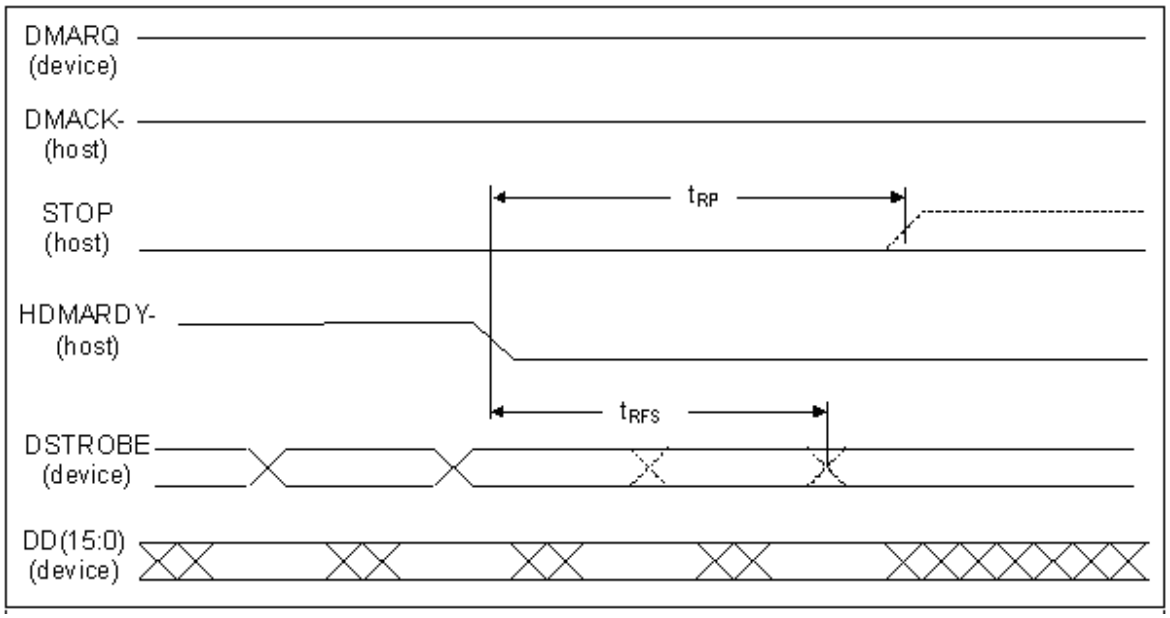
Initiating an Ultra DMA data-in burst



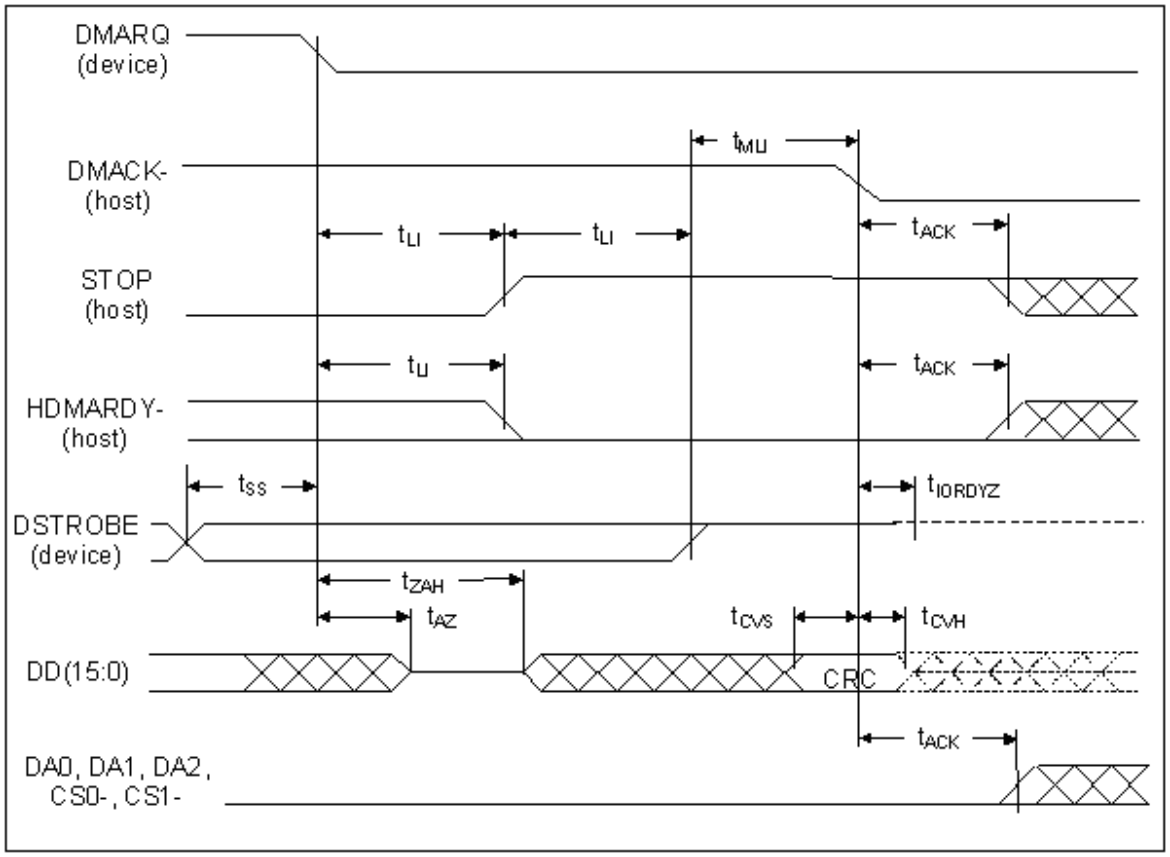
Sustained Ultra DMA data-in burst



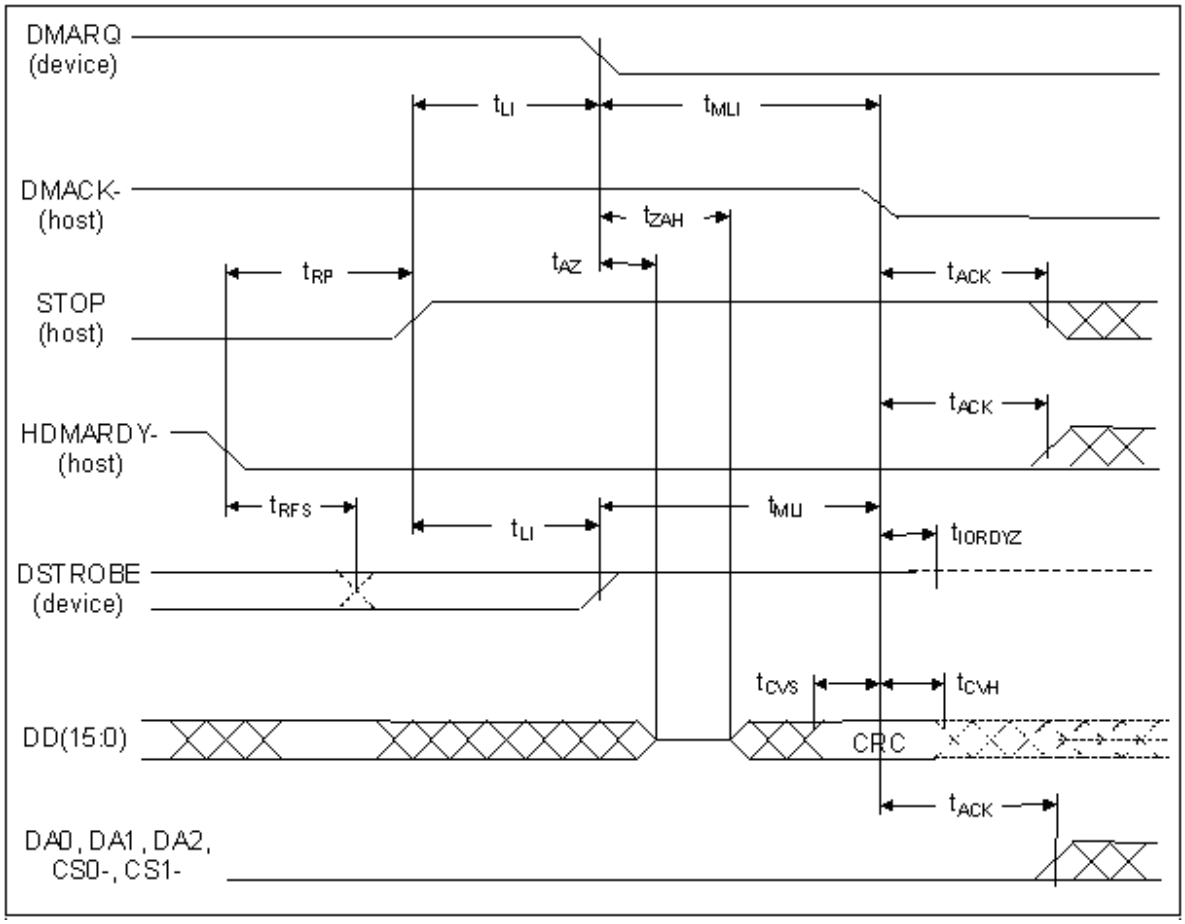
Host pausing an Ultra DMA data-in burst



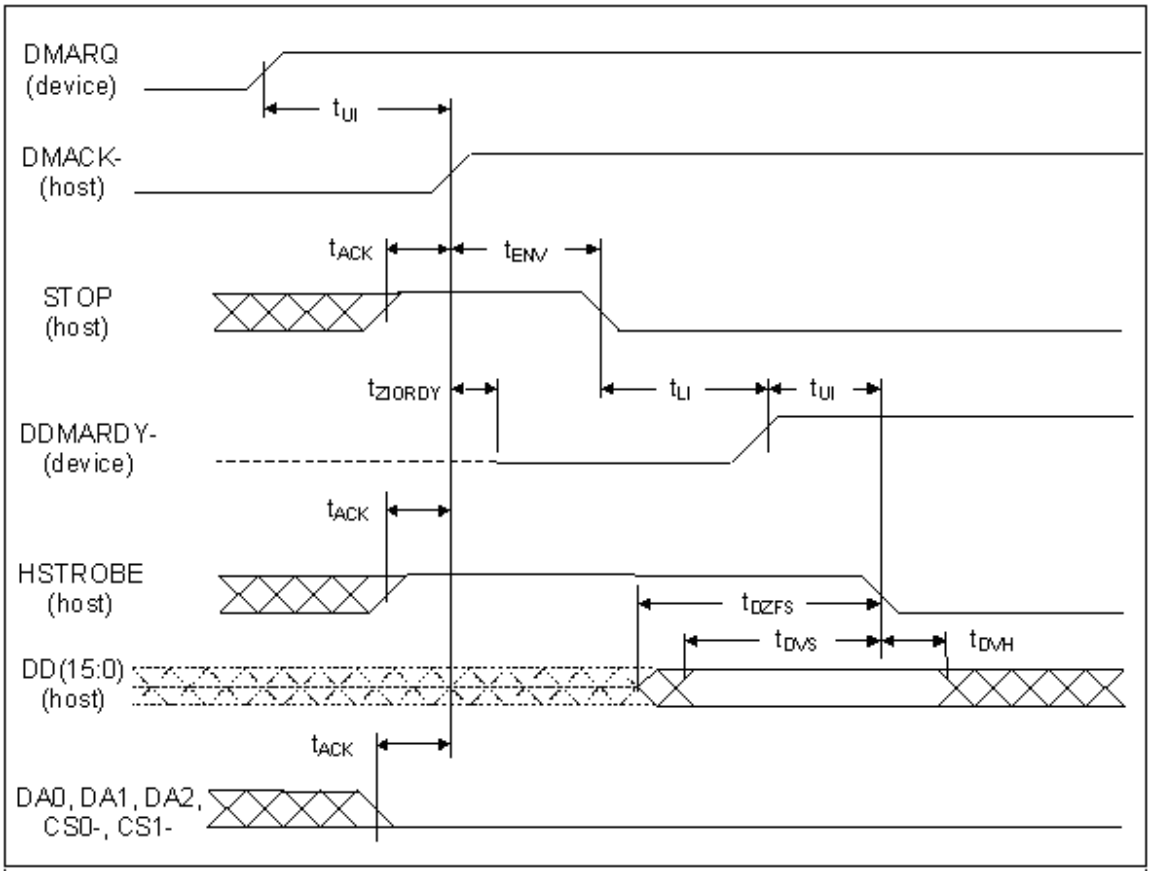
Device terminating an Ultra DMA data-in burst



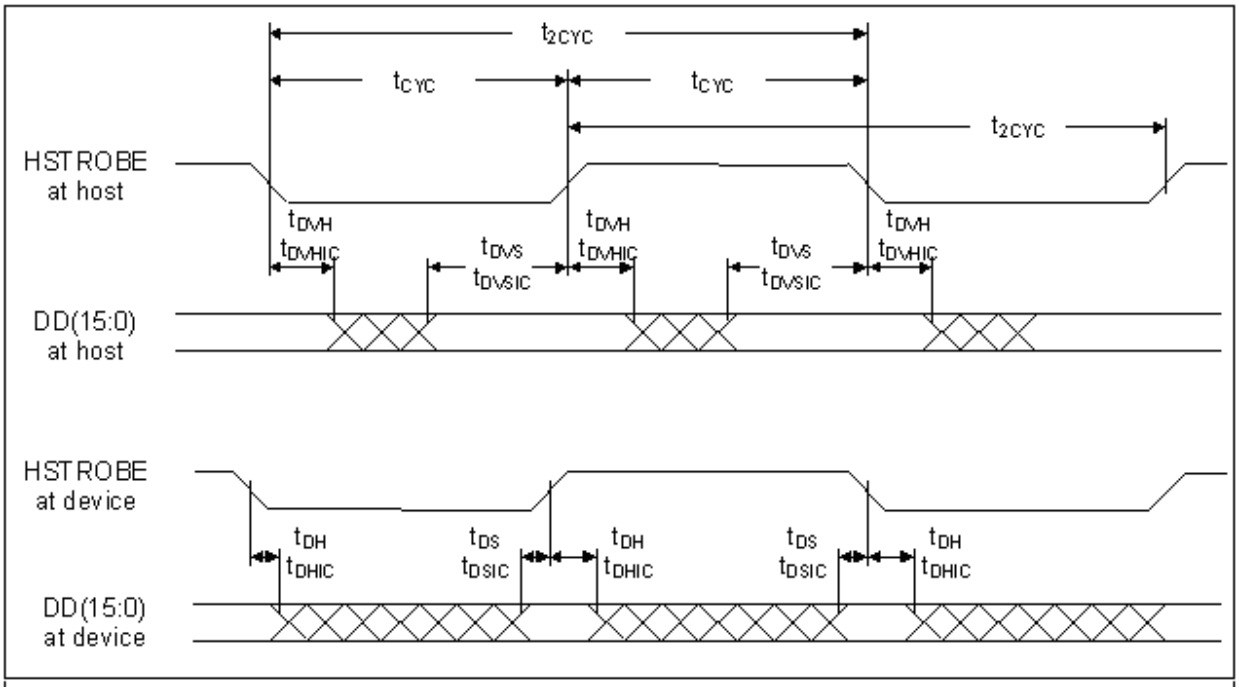
Host terminating an Ultra DMA data-in burst



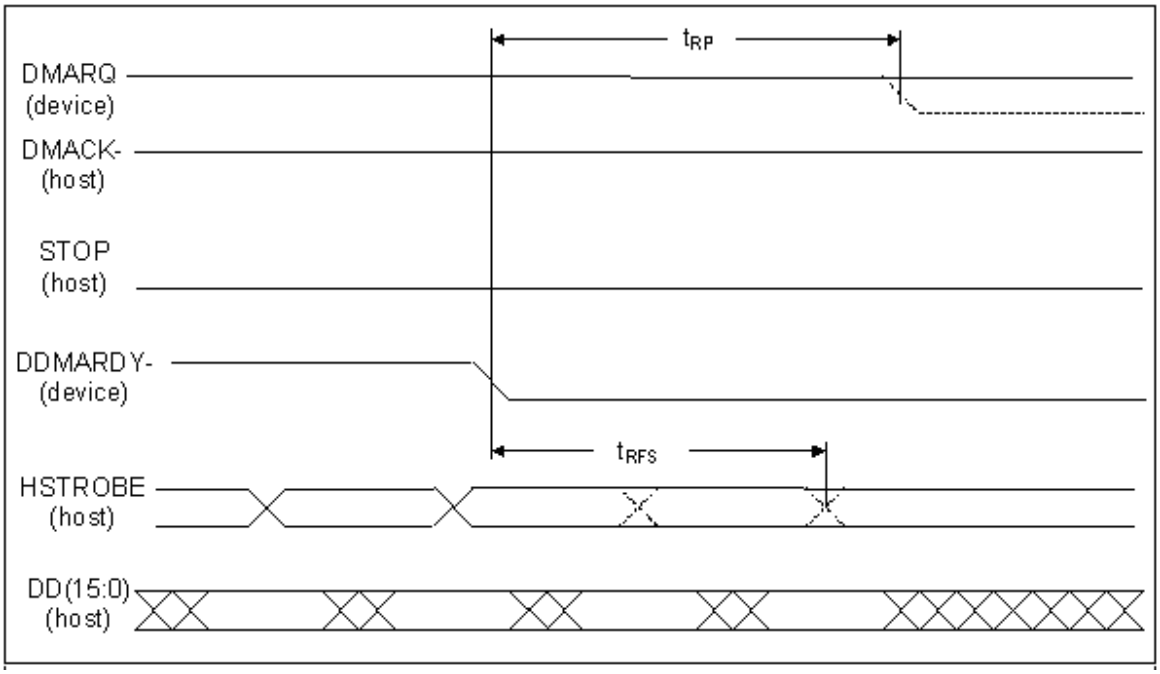
Initiating an Ultra DMA data-out burst



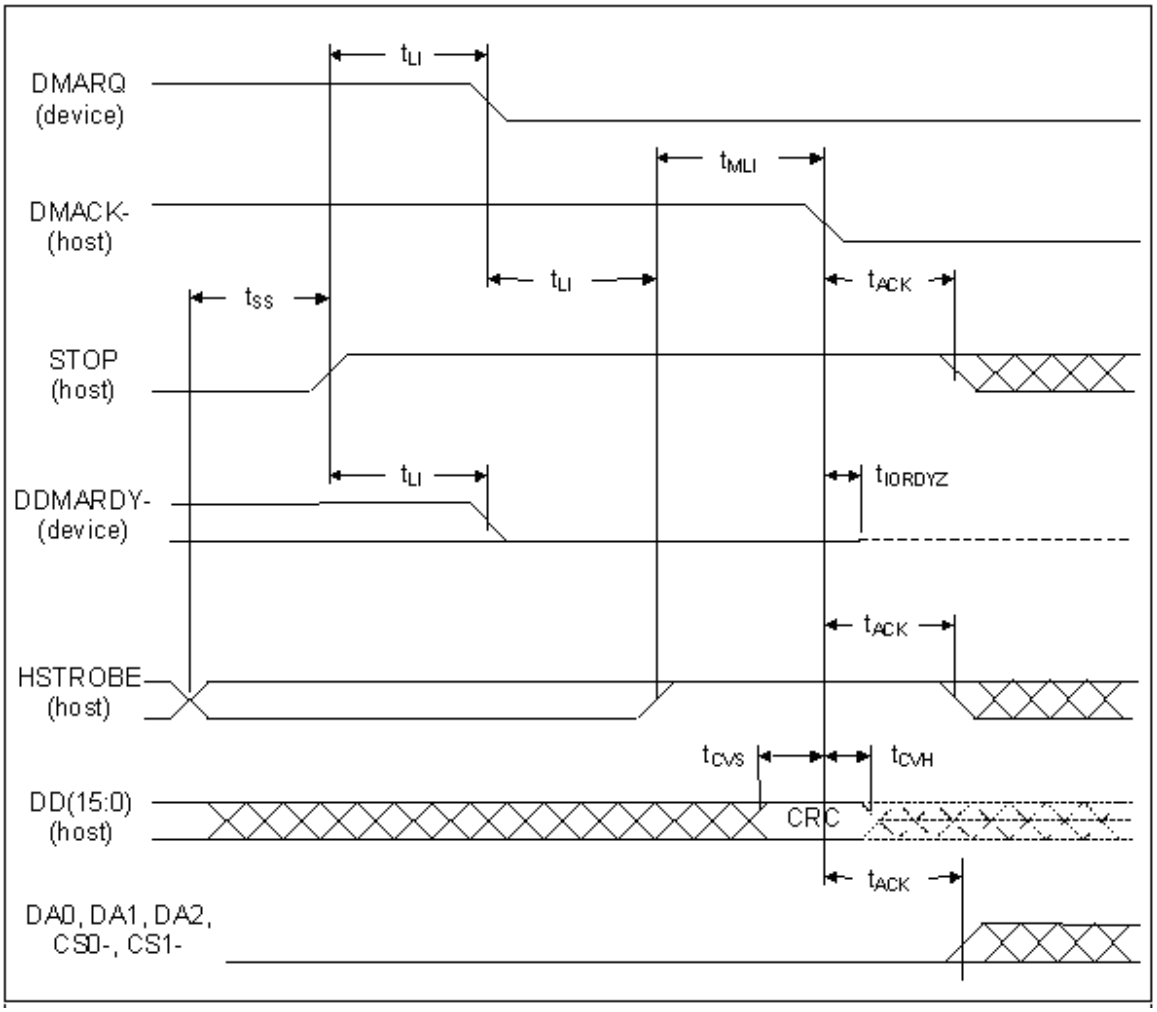
Sustained Ultra DMA data-out burst



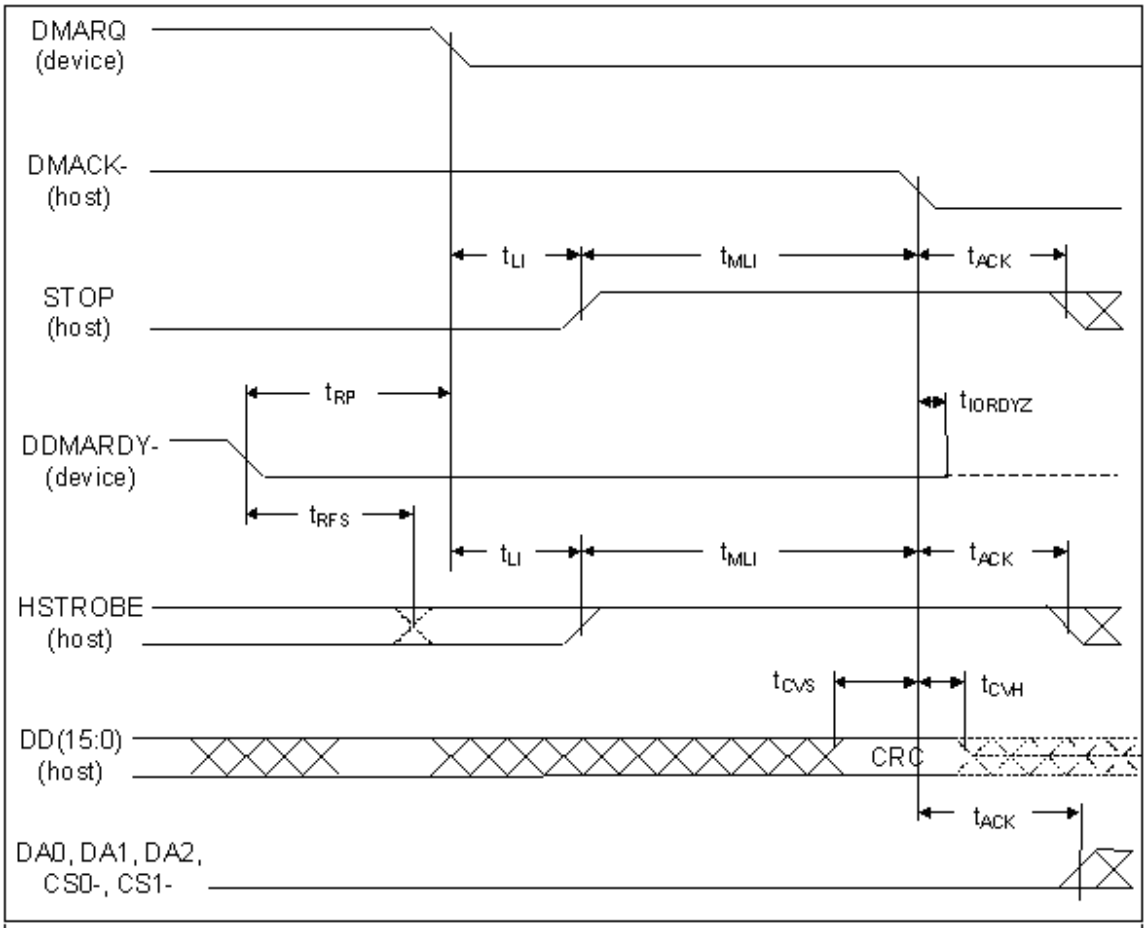
Device pausing an Ultra DMA data-out burst



Host terminating an Ultra DMA data-out burst



Device terminating an Ultra DMA data-out burst



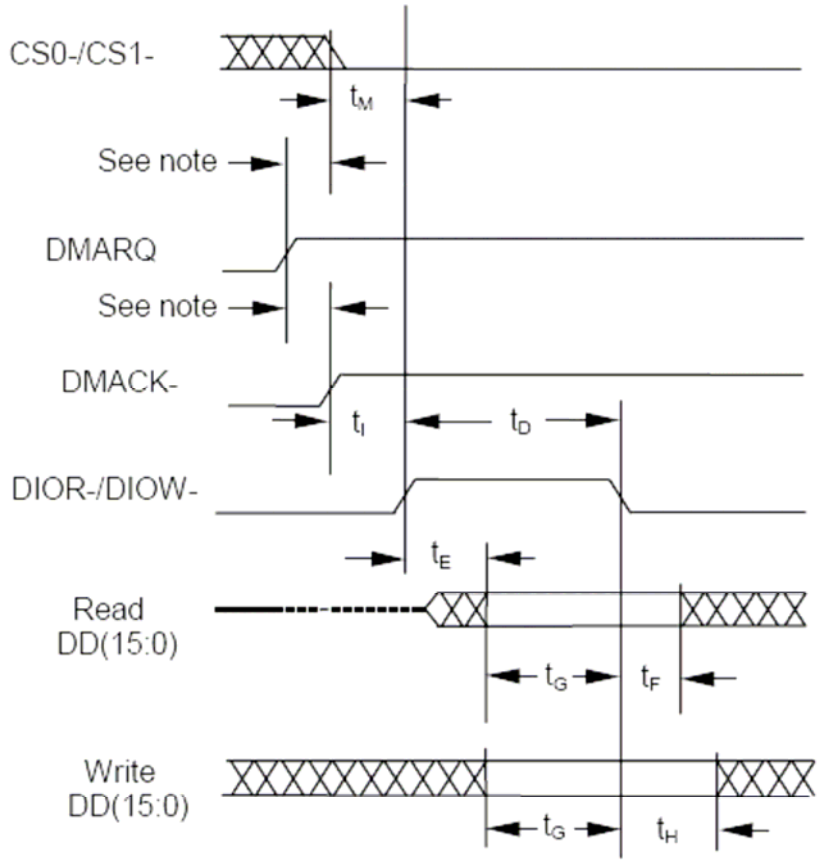
Multiword DMA data transfer

For Multiword DMA modes 1 and above, the minimum value of t0 is specified by word 65 in the IDENTIFY DEVICE parameter list. Table 50 defines the minimum value that shall be placed in word 65. Devices shall power-up with mode 0 as the default Multiword DMA mode.

Multiword DMA timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Note
t_0	Cycle time	(min)	480	150	120	see note
t_D	DIOR-/DIOW- asserted pulse width	(min)	215	80	70	see note
t_E	DIOR- data access	(max)	150	60	50	
t_F	DIOR- data hold	(min)	5	5	5	
t_G	DIOR-/DIOW- data setup	(min)	100	30	20	
t_H	DIOW- data hold	(min)	20	15	10	
t_I	DMACK to DIOR-/DIOW- setup	(min)	0	0	0	
t_J	DIOR-/DIOW- to DMACK hold	(min)	20	5	5	
t_{KR}	DIOR- negated pulse width	(min)	50	50	25	see note
t_{KW}	DIOW- negated pulse width	(min)	215	50	25	see note
t_{LR}	DIOR- to DMARQ delay	(max)	120	40	35	
t_{LW}	DIOW- to DMARQ delay	(max)	40	40	35	
t_M	CS(1:0) valid to DIOR-/DIOW-	(min)	50	30	25	
t_N	CS(1:0) hold	(min)	15	10	10	
t_Z	DMACK- to read data released	(max)	20	25	25	
NOTE – t_0 is the minimum total cycle time, t_D is the minimum DIOR-/DIOW- assertion time, and t_K (t_{KR} or t_{KW}, as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen t_D and/or t_K to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data.						

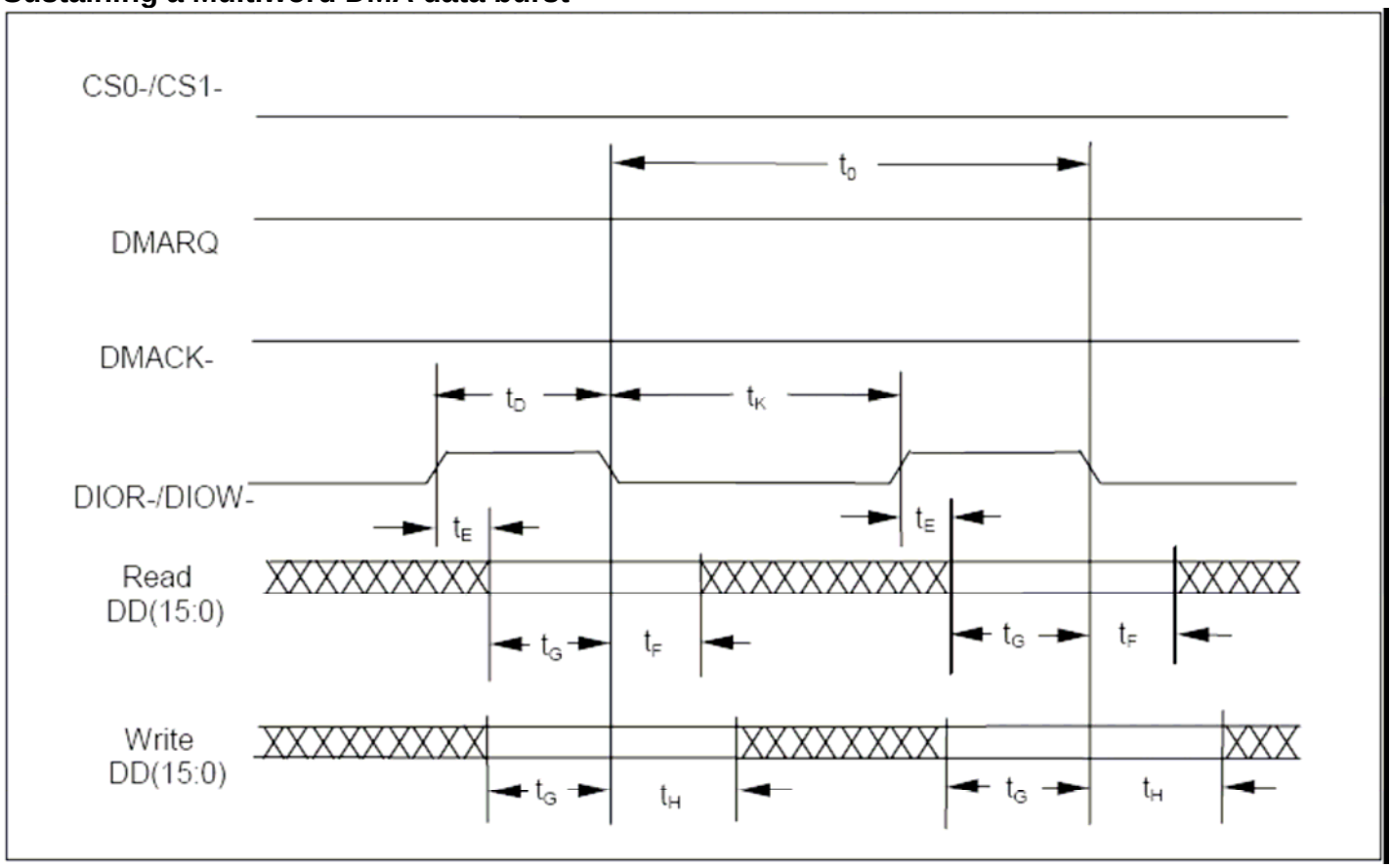
Table – Multiword DMA data transfer

Initiating a Multiword DMA data burst

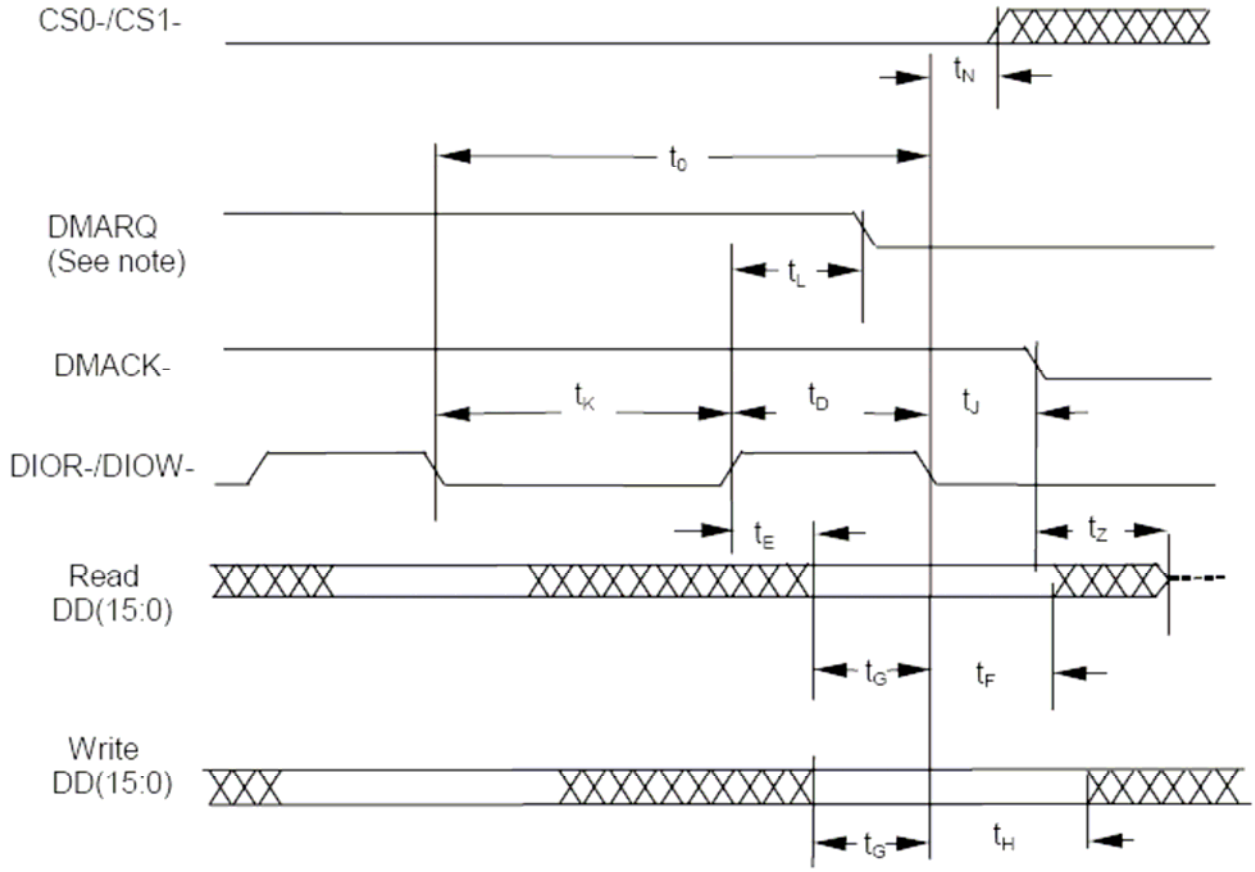


NOTE – The host shall not assert DMACK- or negate both CS0 and CS1 until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK- or the negation of both CS0 and CS1 is not defined.

Sustaining a Multiword DMA data burst

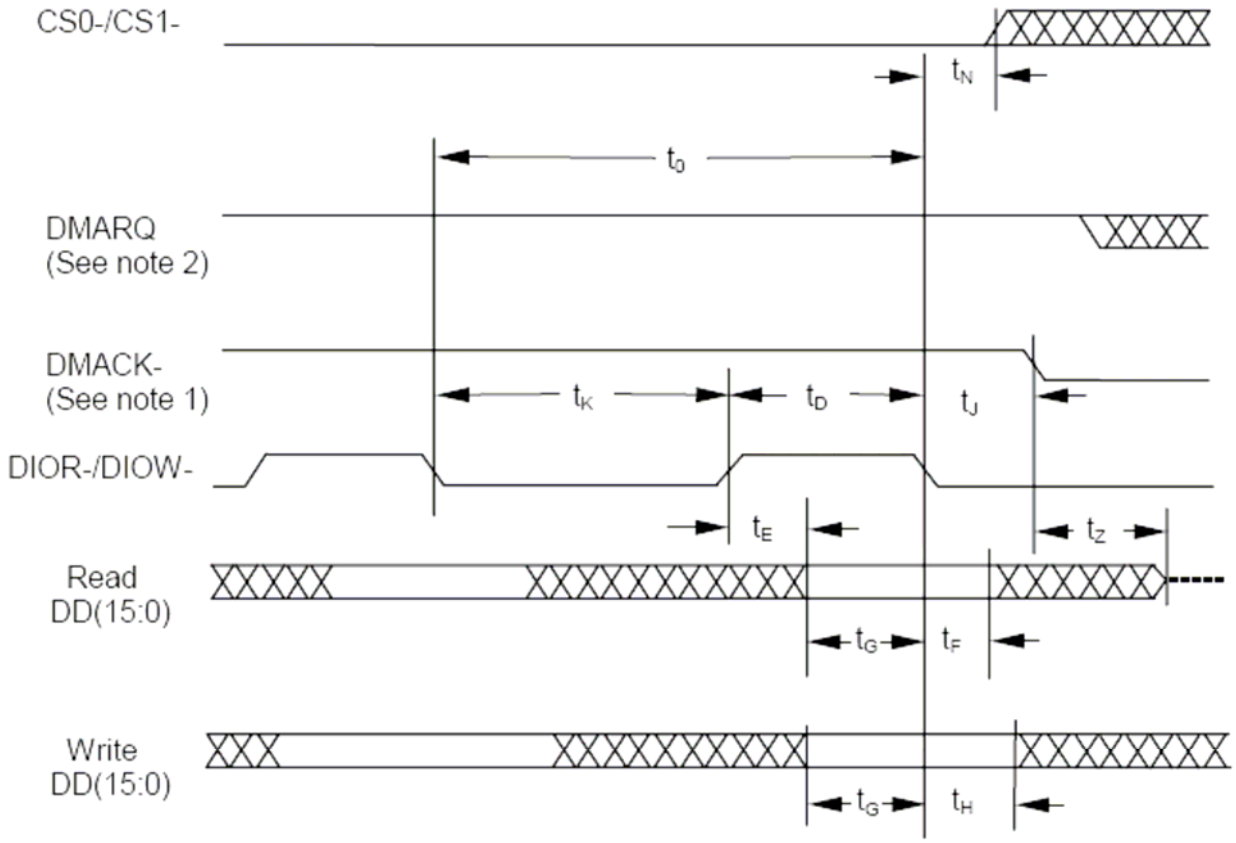


Device terminating a Multiword DMA data burst



NOTE – To terminate the data burst, the Device shall negate DMARQ within t_L of the assertion of the current DIOR- or DIOW- pulse. The last data word for the burst shall then be transferred by the negation of the current DIOR- or DIOW- pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation as shown in figure 66.

Host terminating a Multiword DMA data burst



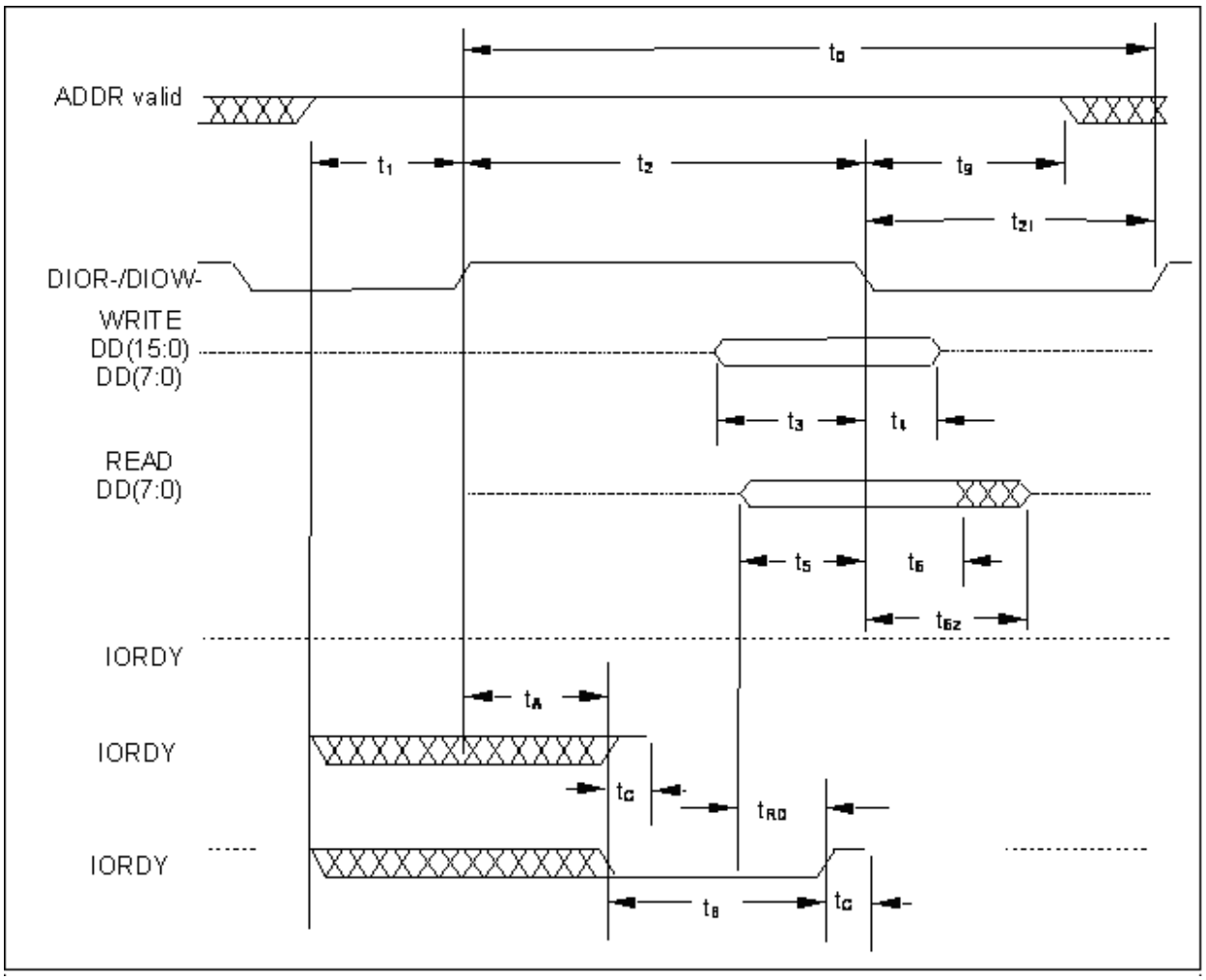
NOTE –
1 To terminate the transmission of a data burst, the host shall negate DMACK- within t_J after a DIOR- or DIOW- pulse. No further DIOR- or DIOW- pulses shall be asserted for this burst.
2 If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK- or may negate DMARQ at any time after detecting that DMACK- has been negated.

PIO data transfer

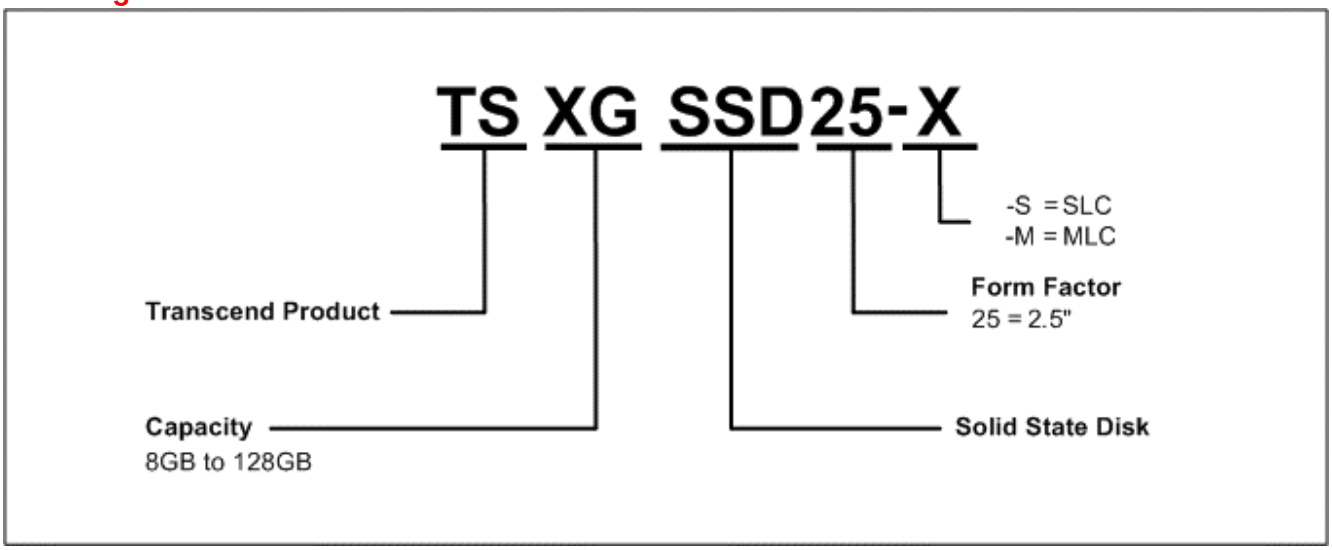
PIO timing requirements

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns
t_0	Cycle time	(min)	600	383	240	180	120
t_1	Address valid to DIOR-/DIOW- setup	(min)	70	50	30	30	25
t_2	DIOR-/DIOW-	(min)	165	125	100	80	70
t_{2i}	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25
t_3	DIOW- data setup	(min)	60	45	30	30	20
t_4	DIOW- data hold	(min)	30	20	15	10	10
t_5	DIOR- data setup	(min)	50	35	20	20	20
t_6	DIOR- data hold	(min)	5	5	5	5	5
t_{6Z}	DIOR- data tristate	(max)	30	30	30	30	30
t_9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	(min)	0	0	0	0	0
t_A	IORDY Setup time		35	35	35	35	35
t_B	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250
t_C	IORDY assertion to release	(max)	5	5	5	5	5

PIO data transfer to/from device



Ordering Information



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